Claims

I Claim:

1. A dc/dc converter comprising:

an inductor coupled to one of a positive output terminal and a positive input terminal;

a first depletion mode compound semiconductor FET coupled to the inductor;

a control circuit coupled to the first depletion mode compound semiconductor FET; and

a capacitor coupled to the positive output terminal and a negative terminal.

2. The dc/dc converter of claim 1 wherein the first depletion mode compound semiconductor FET comprises a GaAs n-channel depletion mode FET.

3. The dc/dc converter of claim 1 further comprising a second depletion mode compound semiconductor FET coupled to the first depletion mode compound semiconductor FET and the control circuit.

4. The dc/dc converter of claim 3 wherein the second depletion mode compound semiconductor FET comprises a GaAs n-channel depletion mode FET.

5. The dc/dc converter of claim 1 further comprising:

a second FET device coupled to the negative terminal and the control circuit; and

a diode having a cathode and an anode, wherein the anode is coupled to the negative terminal and the cathode is coupled between the inductor and the first depletion mode compound semiconductor FET, and wherein the first depletion mode compound semiconductor FET is connected to

the positive input terminal, and wherein the inductor is coupled to a source of the first depletion mode compound semiconductor FET and the positive output terminal to form a buck converter.

6. The dc/dc converter of claim 5 wherein the second depletion mode compound semiconductor FET comprises a depletion mode FET device.

7. The dc/dc converter of claim 5 wherein one of the first and second depletion mode compound semiconductor FETs comprises a GaAs n-channel depletion mode FET.

8. The dc/dc converter of claim 5 wherein both the first and second depletion mode compound semiconductor FETs comprise GaAs n-channel depletion mode FETs.

9. The dc/dc converter of claim 1 further comprising a second FET device coupled to a negative terminal and the control circuit, wherein the inductor is coupled between the positive input terminal and a drain of the first FET device to form a boost converter.

10. The dc/dc converter of claim 9 wherein the second FET comprises a depletion mode FET device.

11. The dc/dc converter of claim 10 wherein one of the first and second depletion mode compound semiconductor FETs comprises a GaAs n-channel depletion mode FET.

12. The dc/dc converter of claim 10 wherein both the first and second depletion mode compound semiconductor FETs comprise GaAs n-channel depletion mode FETs.

13. The dc/dc converter of claim 1 wherein the first depletion mode compound semiconductor FET comprises:

a body of semiconductor material comprising a first conductivity type, wherein the body of semiconductor material has an upper surface and a lower surface opposing the upper surface, wherein the lower surface provides a drain contact;

a first trench formed in the body of semiconductor material and extending from the upper surface, wherein the first trench has a first width, a first depth from the upper surface, first sidewalls, and a first bottom surface;

a second trench formed within the first trench, wherein the second trench has a second width, a second depth from the first surface, second sidewalls and a second bottom surface;

a first source region formed in the body of semiconductor material extending from the upper surface and spaced apart from the first trench; and

a doped gate region formed in at least a portion of the second sidewalls and the second bottom surface, wherein the doped gate region comprises a second conductivity type.

14. The device of claim 13 wherein the body of semiconductor material comprises GaAs.

15. A dc/dc converter network comprising:

a first vertical trench compound semiconductor depletion mode FET device;

an inductor connected to the first FET device and one of a positive input terminal and a positive output terminal;

a gate control device connected to the first FET device; and

a capacitor connected to the positive output terminal.

16. The dc/dc converter network of claim 15 further comprising a second vertical trench compound semiconductor depletion mode FET device connected to a negative terminal, the gate control device and the first vertical trench compound semiconductor depletion mode FET device.

17. The dc/dc converter network of claim 16 wherein one of the first and second vertical trench compound semiconductor depletion mode FET devices comprises a GaAs n-channel depletion mode FET.

18. The dc/dc converter network of claim 16 wherein the first and second vertical trench compound semiconductor depletion mode FET devices comprise GaAs n-channel depletion mode FET devices.

19. A dc/dc converter circuit including:

an inductor connected to one of a positive input terminal and a positive output terminal;

a first GaAs depletion mode vertical FET device connected to the inductor;

a second GaAs depletion mode vertical FET device connected to the first FET device and a negative terminal;

a gate control device connected to the first and second FET devices; and

a capacitor connected to the positive output terminal and the negative terminal.

20. The dc/dc converter circuit of claim 19 wherein one of the first and second GaAs depletion mode vertical FET devices comprises an n-channel device.